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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,483	07/11/2001	Cyril Cabral JR.	YO999-408 CIP	7319

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EXAMINER	
KIELIN, ERIK J	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,483	CABRAL ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-13 and 23-38* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-13 and 23-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04 and 3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 13 May 2004 and the Information Disclosure Statements filed on 17 February 2004 and 8 March 2004.

Information Disclosure Statement

1. The information disclosure statement filed 8 March 2004 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 4, 10, 25, and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24, 28-31 of U.S. Patent No. US 6,503,833 B1 (**Ajamera** et al.). Although the conflicting claims are not identical, they

are not patentably distinct from each other because each teaches the same method of forming the silicide regions by depositing a metal containing silicon followed by equivalent process steps. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa.

4. Claims 1, 4, 10, 25, and 26 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24 and 28-31 of copending Application No. 10/287,476. Although the conflicting claims are not identical, they are not patentably distinct from each other because each teaches the same method of forming the silicide regions depositing a metal containing silicon followed by equivalent process steps. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. Claims 1, 4, 10, 25, and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 27 of U.S. Patent No. US 6,444,578 B1 (**Cabral**, Jr., et al.). Although the conflicting claims are not identical, they are not patentably distinct from each other because each teach the same method of forming the silicide regions depositing a metal containing silicon followed by equivalent process steps.

6. Claims 1, 4, 10, 25, and 26 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 4, 5, and 23 of copending Application No. 10/299,688. Although the conflicting claims are not identical, they are not patentably distinct from each other because each teaches the same method of forming the

silicide regions by depositing a metal containing silicon followed by equivalent process steps. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 1, 4, 10, 25, and 26 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15 and 20 of copending Application No. 09/569,306. Although the conflicting claims are not identical, they are not patentably distinct from each other because each teaches the same method of forming the silicide regions by depositing a metal containing silicon followed by equivalent process steps. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

8. Claims 2-3, 23, and 5-6, 8, 12, 24, and 11, 31, 32, and 27-30, and 33-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24, 28-31 of U.S. Patent No. US 6,503,833 B1 (**Ajamera** et al.) in view of US 5,830,775 (**Maa** et al.).

Ajamera clearly discloses each of the features of the independent claims 1, 4, 10, 25, and 26, as noted above. While **Ajamera** may or may not also teach other features of the claims

depending from said independent claims, **Maa** teaches each of the other features as herein listed below.

Regarding independent claims 1, 4, 13, 25, and 26, **Maa** discloses a method for fabricating a silicide for a semiconductor device, comprising

providing a substrate having a silicon layer (Fig. 1) or a bulk silicon substrate (Fig. 3) (col. 4, lines 13-54);

depositing a metal alloy layer **80** (Fig. 4; col. 2, lines 60-67; col. 4, line 62 to col. 5, line 4);

reacting the metal alloy layer **80** to form a first metal-rich silicide phase layer **90**, using RTA (rapid thermal annealing) (Fig. 5; col. 5, lines 5-65);

selectively etching any unreacted metal alloy while leaving behind the metal-rich silicide **90** (Fig. 6; col. 6, lines 29-49);

depositing a silicon cap layer **110** without using epitaxial processes (Fig. 7; col. 6, line 50 to col. 7, line 15);

reacting the cap layer **110** to form a second silicide phase layer ($CoSi_2$) **122, 124, 126** using RTA (Figs. 8 and 9; col. 7, lines 16-45); and

etching any unreacted silicon cap layer (Fig. 9; col. 7, lines 46-64).

(See also Fig. 10.)

Regarding claims 2 and 3, as noted above, the substrate may be either bulk or SOI.

Regarding claims 5 and 6, the metal alloy may include Co, Ti, or Ni which is 50 Å to 300 Å thick (5 to 30 nm), which anticipates 7 nm to 8 nm (col. 4, line 62 to col. 5, line 4).

Regarding claim 8, as noted above, the reacting of said metal alloy comprises RTA to form a metal-silicon phase by reaction with the underlying bulk silicon substrate; wherein the etching is selective to remove unreacted metal; wherein the silicon cap layer is blanket deposited; and wherein reacting the silicon cap layer is performed by RTA to form a metal di-silicide.

Regarding claim 12, the source/drain regions are shown to be elevated.

Regarding claims 23 and 24, the first silicide phase is the first forming silicide phase.

Regarding claims 27, 29, 31, 33, 35, and 37, the first silicide phase is metal-rich.

Regarding claims 28, 30, 32, 34, 36, and 38, it is seen to be inherent that the metal alloy extends the temperature window in which a silicide metal-rich phase exists, because Applicant indicates that a window is directly related to quantity of metal present in metal alloy. (See Applicant's specification p. 16, lines 3-8.) In other words, the more metal that is present relative to silicon the longer the window. Consequently if an alloy absent silicon is used, the window is a larger than if silicon is present. See *In re Swinhart*, 169 USPQ 226,229 (CCPA 1971) (where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that subject matter shown to be in the prior art does not possess the characteristics relied on) and *In re Fitzgerald*, 205 USPQ 594 (CCPA 1980) (the burden of proof can be shifted to the applicant to show that subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 USC 102 or obviousness under 35 USC 103).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify the claims 24, and 28-31 of **Ajamera** for each of the features in **Maa** because **Maa**

and **Ajamera** are both drawn to the same method for forming shallow junctions on both SOI and silicon substrates, as disclosed and claimed, as is clear from the **Maa** disclosure of each of the features of the independent claims except for the metal containing silicon, a feature which is not critical to the practice of the other features of the dependent claims.

9. Claims 2-3, 23, and 5-6, 8, 12, 24, and 11, 31, 32, and 27-30, and 33-38 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 24 and 28-31 of copending Application No. 10/287,476 in view of **Maa**.

10/287,476 clearly discloses each of the features of the independent claims 1, 4, 10, 25, and 26, as noted above. While 10/287,476 may or may not also teach other features of the claims depending from said independent claims, **Maa** teaches each of the other features as listed above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify the claims 24, and 28-31 of 10/287,476 for each of the features in **Maa** because **Maa** and 10/287,476 are both drawn to the same method for forming shallow junctions on both SOI and silicon substrates as is clear from the **Maa** disclosure of each of the features of the independent claims except for the metal containing silicon, a feature which is not critical to the practice of the other features of the dependent claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. Claims 2-3, 23, and 5-6, 8, 12, 24, and 11, 31, 32, and 27-30, and 33-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 27 of U.S. Patent No. US 6,444,578 B1 (**Cabral**, Jr., et al.) in view of **Maa**.

Cabral clearly discloses each of the features of the independent claims 1, 4, 10, 25, and 26, as noted above. While **Cabral** may or may not also teach other features of the claims depending from said independent claims, **Maa** teaches each of the other features as listed above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify the claims 1 and 27 of **Cabral** for each of the features in **Maa** because **Maa** and **Cabral** are both drawn to the same method for forming shallow junctions on both SOI and silicon substrates, as is clear from the **Maa** disclosure of each of the features of the independent claims except for the metal containing silicon, a feature which is not critical to the practice of the other features of the dependent claims.

11. Claims 2-3, 23, and 5-6, 8, 12, 24, and 11, 31, 32, and 27-30, and 33-38 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 4, 5, and 23 of copending Application No. 10/299,688 in view of **Maa**.

10/299,688 clearly discloses each of the features of the independent claims 1, 4, 10, 25, and 26, as noted above. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa. While 10/299,688 may or may not also teach other features of the claims depending from said independent claims, **Maa** teaches each of the other features as listed above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify the claims 1, 4, 5, and 23 of 10/299,688 for each of the features in **Maa** because **Maa** and 10/299,688 are both drawn to the same method for forming shallow junctions on both SOI and silicon substrates, as is clear from the **Maa** disclosure of each of the features of the independent claims except for the metal containing silicon, a feature which is not critical to the practice of the other features of the dependent claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

12. Claims 2-3, 23, and 5-6, 8, 12, 24, and 11, 31, 32, and 27-30, and 33-38 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15 and 20 of copending Application No. 09/569,306 in view of **Maa**.

09/569,306 clearly discloses each of the features of the independent claims 1, 4, 10, 25, and 26, as noted above. Note that a "metal-silicon mixture" is equivalent to a "metal containing silicon." The patent cannot be infringed without also infringing the application and vice versa. While 09/569,306 may or may not also teach other features of the claims depending from said independent claims, **Maa** teaches each of the other features as listed above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to modify the claims 15 and 20 of 09/569,306 for each of the features in **Maa** because **Maa** and 09/569,306 are both drawn to the same method for forming shallow junctions on both SOI and silicon substrates, as is clear from the **Maa** disclosure of each of the features of the independent

claims except for the metal containing silicon, a feature which is not critical to the practice of the other features of the dependent claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

The rejection of the claims over Maa in view of Cabral is withdrawn. While Maa teaches each of the features of the claimed invention except for depositing, *inter alia*, metals, "alloyed combinations of suitable silicidation materials" (Maa, col. 5, first full sentence) containing silicon, Examiner is of the opinion that the use of specifically a metal containing silicon would be, at best, obvious to try, for reasons indicated by Applicant on pp. 15 to 23. One particular reason is that, in the Cabral reference, the metal containing silicon (titanium and silicon) is used to avoid plural annealing steps. Maa carries out plural annealing steps, which contradicts at least one reason for using the metal containing silicon (titanium and silicon) in Cabral.

Nonetheless, Examiner expressly disagrees with Applicant in regard to the following. Applicant argues, yet again, that Maa does not teach a metal alloy. Applicant blatantly and intentionally ignores the facts of record in spite of the numerous times that this fact has been pointed out to Applicant. **Maa expressly indicates that a METAL ALLOY is deposited on the substrate, in the paragraph bridging cols. 4 to 5 --specifically at col. 5, first whole sentence,** stating,

> "Referring to FIG. 4, following the formation of gate structure 30 and the ion implantation steps creating source and drain electrode regions 46, 48, a layer of silicidation material 80 is deposited on substrate 10. Silicidation material thus covers the single-crystal silicon of source/drain

> electrodes 46, 48. Suitable materials for use in siliciding semiconductor electrodes include refractory metals and noble metals. Examples of the silicidation material includes Co, Ti, Ni, W, Pt, Pd, Mo, and Ta. Layer 80 preferably has a thickness generally in the range of 50 Å to 300 Å. Layer 80 is either a uniform layer of a single metal, for example cobalt, or, alternatively, is made up of more than one layer of silicidation material. For example, layer 80 might include a lower layer of Ti, and an upper layer of Co. Other layered or **alloyed** combinations of suitable silicidation materials for use in creating silicide contacts on semiconductor electrodes will occur to those skilled in the art."

Accordingly, Applicant's *ad naseum* insistence that Maa does not teach depositing a metal alloy is wholly without merit. It is also noted with interest, that **yet again**, Applicant, in the section entitled "III. The Prior Art Rejections" on p. 13, of the paper filed 13 May 2004, quotes the above excerpt from Maa **up to the last sentence** of the above paragraph, ignoring that Maa states the word "alloyed combinations." Examiner is perplexed at Applicant's continued insistence that metal alloys and other "alloyed combinations" are not disclosed in Maa, in spite of the **numerous** times which Examiner has pointed out this feature in Maa.

Moreover, Applicant has narrowed the claims in attempts to overcome the prior art. Originally Applicant claimed a metal and a metal alloy. The limitation, "metal containing silicon," was not added until the provision of prior art anticipating the claims. Applicant's numerous amendments to the claims makes claim that the claims have been narrowed with respect to the material being deposited to form the silicide layer. Accordingly, the instant claims are **not** entitled to the doctrine of equivalents with respect to metal and metal alloy materials being deposited from which the silicide is made, in accordance with precedent.

Applicant's arguments regard the double patenting rejections are noted. Applicant argues that the applied references do not teach "depositing a metal containing silicon on a silicon substrate." While it is noted that the claims in the applied references over which the double patenting rejection are may state "a semiconductor substrate," a silicon substrate is a semiconductor substrate. Accordingly, the claims are still obvious over the applied references. Also, depositing a metal containing silicon is very clearly claimed in each of the applied reference claims regardless of the manner by which the metal containing silicon is recited. Accordingly, these arguments are not found, at all, persuasive.

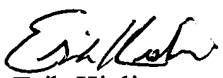
Conclusion

This action is made non-final to give Applicant the opportunity to respond to the new grounds of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
21 May 2004